

Docket No.: 67161-039

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
	:	
Hideto HIDAKA	:	
	:	
Serial No.:	:	Group Art Unit:
	:	
Filed: July 10, 2003	:	Examiner:
	:	
For: SEMICONDUCTOR MEMORY DEVICE WITH MAGNETIC DISTURBANCE REDUCED		

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

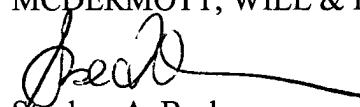
The relevance of JP 2002-170375 is discussed in the present specification.

Serial No.:

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY


Stephen A. Becker

Registration No. 26,527

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:km
Facsimile: (202) 756-8087
Date: July 10, 2003

INFORMATION DISCLOSURE CITATION IN AN APPLICATION				ATTY. DOCKET NO. 67161-039		SERIAL NO.		
(PTO-1449)				APPLICANT Hideto HIDAKA				
				FILING DATE July 10, 2003		GROUP		
U.S. PATENT DOCUMENTS								
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
	A1	US	2002/0172073	11/21/2002	HIDAKA			
		US	10/327,888	12/26/2002	HIDAKA			
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FOREIGN PATENT DOCUMENTS								
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
							Yes	No
		JP	2002-170375	06/14/2002	HIRAI		abstract	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.						
		SCHEUERLEIN, et al. "A 10ns Read and Write Non-Volatile Memory Array Using a Magnetic Tunnel Junction and FET Switch in Each Cell" IEEE International Solid-State Circuits Conference (2000) TA 7.2						
		DURLAM, et al. "Nonvolatile RAM Based on Magnetic Tunnel Junction Elements" IEEE International Solid-State Circuits Conference (2000) TA 7.3						
		NAJI, et al. "A 256kb 3.0V 1T1MJT Nonvolatile Magnetoresistive RAM" IEEE International Solid-State Circuits Conference (2000) TA 7.6						
EXAMINER				DATE CONSIDERED				

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.